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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,265	02/07/2002	Jun Dong Kim	P67585US0	6688

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	10/067,265	KIM ET AL.
	Examiner	Art Unit
	Asok K. Sarkar	2829

-- The MAILING DATE of this c mmunicati n appears on the cover she t with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford, US 2002/0187434 in view of Kashihara, US 6,458,284 and Lin, US 6,150,263.

Regarding claim 1, Blatchford teaches a method of photolithographic process (forming a photoresist film and etching the photoresist film using a photolithography process) prior to transfer of the features into an underlying substrate (see paragraphs 9 and 19) in which he forms the first mask pattern 120 on the substrate 110 in such a manner that the desired region of the substrate is exposed with reference to Fig. 3A and isotropic etching (see paragraph 12) the first mask pattern to form the second mask pattern with reference to Fig. 3B and Fig. 2. Removal of the second mask pattern is inherent in the process since during the formation of the device the mask patterns are removed. Blatchford also teaches transfer of the developed pattern into the underlying substrate using conventional expedients in paragraph 13.

Blatchford fails to teach (1) successively forming a conducting layer and a insulating layer on a substrate to form a bit line, (2) locating the taught the first mask pattern on an insulating layer, (3) using dry etching to form the second mask pattern, (4) removing the insulating layer by first anisotropic dry etching using the second mask pattern, and (5) etching the conducting layer by a second anisotropic dry etching using the remaining insulating layer.

Kashihara teaches forming (1) bit lines by successively forming a conducting layer 2 and an insulating/hard mask layer 1a with reference to Fig. 2 in column 6, lines 6 – 27. Kashihara teaches hard mask layer of insulating silicon oxide in column 3, line 47 and therefore forming the first mask pattern on the insulating layer to expose the insulating layer. Kashihara teaches (3) isotropic dry etching the mask pattern of Fig. 10 to provide the mask pattern of smaller size in column 9, lines 26 – 67. Kashihara teaches (part of item 5) etching the conducting layer 2, using the remaining hard mask/insulating layer with reference to Fig. 11.

Kashihara fails to teach (4) removing the insulating layer by first anisotropic dry etching and (5) etching the conducting layer by a second anisotropic dry etching.

Lin teaches a similar method as Kashihara to fabricate small dimension wires for bit lines (see column 3, line 23) with reference to Figs. 1A – 1D. Lin teaches (5) anisotropic dry etching for the conducting layer using an etched mask layer of conductive material 140b with respect to Fig. 1D in column 3, lines 8 – 20. Lin fails to teach (4) removing the insulating layer by first anisotropic dry etching.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to apply the photolithographic process taught by Blatchford to the substrates by successively forming the conducting layer and the insulating layer (1) in order to form the bit lines of smaller dimension since Kashihara teaches the advantages of using the insulating layer on the conducting layer to overcome the limitations of thin photoresist layer in order to apply Blatchford's process more effectively.

It would have been obvious to one with ordinary skill in the art at the time of the invention when Blatchford's process is applied to reduce the size of the conductive line with the insulating layer on top, the first mask pattern will be formed on the insulating layer (2).

It would have been obvious also to one with ordinary skill in the art at the time of the invention to use dry etching to form the second mask pattern (3) since etching processes can be either dry or wet isotropic etching process as taught by Kashihara.

Furthermore, it would have been obvious also to one with ordinary skill in the art at the time of the invention to use anisotropic etching of the insulating and the conducting layers (4 and 5) as taught by Lin for the conducting layer, since etching is carried out to define a shape on a layer in the depth direction for the lower conducting layer using the second mask pattern and the etching processes can be either dry or wet isotropic etching process as taught by Kashihara.

Regarding claim 12, Kashihara teaches hard mask layer of oxide and nitride in column 3, line 26.

Regarding claim 13, Lin teaches conducting layer of tungsten silicide in column 2, line 50.

4. Claims 5 – 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford, US 2002/0187434 in view of Kashihara, US 6,458,284 or Lin, US 6,150,263 as applied to claims 1 - 3 above, and further in view of Wolf and Tauber, "Silicon processing for the VLSI Era, Vol. 1", Chapter 16, p 539, Lattice Press, CA (1986).

Blatchford teaches etching rate of less than 3000 Angstrom in paragraph 43.

Blatchford in view of Kashihara or Lin fails to teach isotropic dry etching process using, microwave power at a selected range, oxygen gas at a selected range of flow rate, CF_4 gas, gas pressure inside the etching chamber and the etching rate.

Wolf and Tauber teaches throughout chapter 16 various ways of dry etching can be applied to different materials including the use of microwave energy, CF_4 gas and oxygen for etching resist materials (Organic Films in Page 564), various equipments and process control throughout the chapter.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control these parameters during the etching process through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05).

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford, US 2002/0187434 in view of Kashihara, US 6,458,284, Lin, US 6,150,263

and Wolf and Tauber, "Silicon processing for the VLSI Era, Vol. 1", Chapter 16, p 539, Lattice Press, CA (1986).

Blatchford teaches a method of photolithographic process (forming a photoresist film and etching the photoresist film using a photolithography process) prior to transfer of the features into an underlying substrate in which he forms the first photoresist pattern 120 on the substrate 110 in such a manner that the desired region of the substrate is exposed with reference to Fig. 3A and partially removing by isotropic etching the first photoresist mask pattern to form the second photoresist mask pattern with reference to Fig. 3B and Fig. 2. Removal of the second photoresist mask pattern is inherent in the process.

Blatchford teaches photoresist pattern having a width of at least 0.14 and having the second photoresist mask pattern to have the feature width of the size of less than 0.1μ in paragraph 27.

Blatchford fails to teach successively forming a conducting layer and a insulating layer on a substrate to form a bit line, forming the first photoresist pattern on the insulating layer to expose the insulating layer, isotropic dry etching the first mask pattern by supplying oxygen gas at a specific flow rate using microwave energy at a power less than 400W and at a pressure of 600 – 1000 mT, removing a portion of the insulating layer by first anisotropic dry etching using the second photoresist mask pattern to form a hard mask, removing the second photoresist pattern and etching the conducting layer by a second anisotropic dry etching using the hard mask.

Kashihara teaches forming bit lines by forming a conducting layer 2 and a hard mask layer 1a with reference to Fig. 2 in column 6, lines 6 – 27. Kashihara teaches hard mask layer of insulating silicon oxide in column 3, line 47 and therefore forming the first photoresist pattern on the insulating layer to expose the insulating layer. Kashihara teaches isotropic dry etching the mask pattern of Fig. 10 to provide the mask pattern of smaller size in column 9, lines 26 – 67. Kashihara teaches various plasma dry etching equipment that uses microwave energy in column 8, lines 40 – 52. Kashihara teaches etching the conducting layer 2, using the remaining hard mask/insulating layer with reference to Fig. 11.

Kashihara fails to teach removing the insulating layer by first anisotropic dry etching and etching the conducting layer by a second anisotropic dry etching.

Lin teaches a similar method as Kashihara to fabricate small dimension wires for bit lines (see column 3, line 23) with reference to Figs. 1A – 1D. Lin teaches anisotropic dry etching for the conducting layer using an etched mask layer of conductive material 140b with respect to Fig. 1D in column 3, lines 8 – 20. Lin fails to teach removing the insulating layer by first anisotropic dry etching.

Kashihara and Lin fail to teach isotropic dry etching process using, microwave power at a selected range, oxygen gas at a selected range of flow rate and gas pressure inside the etching chamber.

Wolf and Tauber teaches throughout chapter 16 various ways of dry etching can be applied to different materials including the use of microwave energy, oxygen for etching resist materials (Organic Films in Page 564), various equipments and process

control throughout the chapter so that optimum device features can be reproducibly made.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to apply the photolithographic process taught by Blatchford to the substrates containing the conducting layer and the insulating layer in order to form the bit lines of smaller dimension since Blatchford, Kashihara and Lin teach the method of feature size reduction to overcome the limitation of the photolithographic process. Blatchford's process can be modified by using the insulating layer on the conducting layer to overcome the limitations of thin photoresist layer as taught by Kashihara and when Blatchford's process is applied to reduce the size of the conductive line with the insulating layer on top, anisotropic etching of both layers will be needed as taught by Lin for the conducting layer, since etching is carried out to define a shape on a layer in the depth direction and the etching processes can be either dry or wet isotropic etching process as taught by Kashihara.

Similarly, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the process parameters during the dry etching process in a microwave plasma equipment through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) for the resultant manufactured devices.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 703 308 2521. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703 308 1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703 308 7722 for regular communications and 703 308 7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 4918.

Asok K. Sarkar
June 4, 2003

EVAN PERT